A cloud-accessible four-qubit electron spin QPU in a 300 mm metal-oxide-semiconductor process

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Abstract—We present a cloud-accessible electron spin-qubit quantum processor manufactured in an industrial 300 mm silicon metal-oxide-semiconductor process. Four single-electron spin qubits form a linear array with controllable nearest-neighbour exchange coupling; the unit cell can be tiled without design modification, providing a direct path to larger processors. The system is installed at the UK's National Quantum Computing Centre, where automated calibration maintains operation with minimal human input and users submit circuits through industry-standard frameworks including Qiskit and Cirq. This deployment is a prototype for future HPC integration. Single-qubit gates are driven by magnetic resonance; two-qubit CPhase gates use electrically modulated exchange coupling. Single-shot readout via a parallel array of charge sensors achieves fidelities above 99% in under 10 µs and supports mid-circuit measurement. We demonstrate two applications: a variational quantum eigensolver determining the equilibrium bond length of molecular hydrogen, and stabiliser measurements demonstrating the building block of quantum error correction.

Keywords—silicon spin qubits, 300 mm CMOS manufacturing, cloud quantum computing, automated calibration, quantum error detection, HPC integration

I. Introduction

For quantum computing to be viable, qubits must be manufactured using processes that can scale to the sizes required for fault tolerance. Electron spin qubits in silicon metal-oxide-semiconductor (MOS) devices are well suited to this requirement: they are small and they can be manufactured on the same 300 mm processes used by the semiconductor industry. Equally, these devices must be operated as computing systems rather than as physics experiments, with remote access, standard programming interfaces and minimal human input.

We present QM One, a full-stack quantum processing unit (QPU) based on four single-electron spin qubits manufactured using imec's 300 mm silicon MOS process. The system is installed at the UK's National Quantum Computing Centre (NQCC) and is operated entirely via a cloud interface. This deployment is a prototype for future HPC integration.

II. A Scalable Unit Cell

The QPU consists of two parallel linear arrays of gate-defined quantum dots. Qubits are defined in the top array, with controllable nearest-neighbour exchange coupling between them; single-electron-transistor charge sensors in the bottom array provide readout. These arrays can be tiled to support increasing QPU sizes without design modifications.

Single-qubit gates are performed via electron spin resonance with a mean duration of 1.1 µs. The qubit resonance frequencies are separated by less than 2 MHz, and the resulting crosstalk is mitigated via pulse engineering. Two-qubit CPhase gates are available between all nearest-neighbour pairs, implemented as geometric phase gates via electrically modulated exchange, with a mean duration of 426 ns. Randomized benchmarking on all four qubits gives an average single-qubit gate fidelity of 99%. Readout is single-shot, with fidelities above 99% in under 10 µs, and supports mid-circuit measurement.

III. Cloud Access and Automated Calibration

QM One is operated as a service rather than an experiment. Users submit quantum circuits via a cloud interface that accepts industry-standard frameworks including Qiskit and Cirq; jobs are queued, executed and returned without intervention from on-site staff.

The device parameters drift over time, so maintaining the system requires regular recalibration. Automated calibration routines monitor the device and retune the relevant control parameters, including initialisation and readout voltage sequences, single-qubit gate frequencies and amplitudes, and two-qubit gate voltages and timings. This keeps the QPU operational with minimal human input, which will be essential when QPUs are deployed in HPC centres where dedicated expert attention per device is not practical.

IV. Application Demonstrations

We benchmark the deployed system with two applications, both submitted via the cloud interface.

The first is a variational quantum eigensolver used to model molecular hydrogen. We use a chemically inspired ansatz with optimised compilation, and estimate the expectation value of each term in the Hamiltonian from the measured output distributions. The resulting energy curve gives the equilibrium bond length of H_2. This demonstration runs the full hybrid quantum-classical loop of parameterised circuit submission, execution and classical optimisation.

The second is quantum error detection. We run repeated XX and ZZ stabiliser cycles, in which the parity of a pair of data qubits is projected onto a neighbouring ancilla via mid-circuit measurement. Using these cycles we generate entangled states via stabiliser measurement, demonstrate noise purification in which injected bit-flip errors are reduced through syndrome post-selection, and perform logical encoding in a two-data-qubit subspace. The circuits take advantage of the qubit topology, including data-on-data gates in the spirit of recent code morphing ideas. To our knowledge this is the first demonstration of quantum error detection in a silicon MOS device.

V. Outlook

The poster presents the device architecture, the cloud and calibration stack, and both demonstrations, with performance

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data from the deployed system. Future work targets larger tiled arrays, cryogenic CMOS control electronics and standard interfaces to HPC resource managers, allowing silicon QPUs to be deployed alongside classical accelerators in hybrid facilities.